

L Number	Hits	Search Text	DB	Time stamp
1	0	bernstein-k\$,in.	USPAT; EPO; JPO; DERWENT	2004/06/11 13:29
2	108	bernstein-k\$.in.	USPAT; EPO; JPO; DERWENT	2004/06/11 13:56
3	761	LSSD or (level adj2 sensitive adj2 scan adj2 design)	USPAT; EPO; JPO; DERWENT	2004/06/11 13:57
4	0	(LSSD or (level adj2 sensitive adj2 scan adj2 design)) and bernstein-k\$.in.	USPAT; EPO; JPO; DERWENT	2004/06/11 13:57
5	45	(LSSD or (level adj2 sensitive adj2 scan adj2 design)) and (stress\$4 or burn-in or (reliability adj2 test))	USPAT; EPO; JPO; DERWENT	2004/06/11 13:58
6	30	(LSSD or (level adj2 sensitive adj2 scan adj2 design)) and (stress\$4 or burn-in or (reliability adj2 test)) and (VCC or VDD or voltage\$1 or (power adj2 rail\$1))	USPAT; EPO; JPO; DERWENT	2004/06/11 13:59
7	27	(LSSD or (level adj2 sensitive adj2 scan adj2 design)) and (stress\$4 or burn-in or (reliability adj2 test)) and (VCC or VDD or voltage\$1 or (power adj2 rail\$1)) and (flip-flop\$1 or latch\$3)	USPAT; EPO; JPO; DERWENT	2004/06/11 14:00
8	27	(LSSD or (level adj2 sensitive adj2 scan adj2 design)) and (stress\$4 or burn-in or (reliability adj2 test)) and (VCC or VDD or voltage\$1 or (power adj2 rail\$1)) and (flip-flop\$1 or latch\$3) and (logic or core or combinatorial)	USPAT; EPO; JPO; DERWENT	2004/06/11 14:00
9	27	(LSSD or (level adj2 sensitive adj2 scan adj2 design)) and (stress\$4 or burn-in or (reliability adj2 test)) and (VCC\$1 or VDD\$1 or voltage\$1 or (power adj2 rail\$1)) and (flip-flop\$1 or latch\$3) and (logic or core or combinatorial)	USPAT; EPO; JPO; DERWENT	2004/06/11 14:01
10	36	(LSSD or (level adj2 sensitive adj2 scan adj2 design)) and (stress\$4 or burn-in or (reliability adj2 test)) and (VCC\$1 or VDD\$1 or voltage\$1 or (power adj2 rail\$1) or de-power\$ or power\$4) and (flip-flop\$1 or latch\$3) and (logic or core or combinatorial)	USPAT; EPO; JPO; DERWENT	2004/06/11 14:02



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1 Analysis of grouped and censored data from step-stress life test

Chengjie Xiong; Ming Ji;

Reliability, IEEE Transactions on , Volume: 53 , Issue: 1 , March 2004

Pages:22 - 28

[Abstract] [PDF Full-Text (224 KB)] IEEE JNL

2 Selection of display devices used at man-machine interfaces based on human factors

Muraoka, T.; Ikeda, H.;

Industrial Electronics, IEEE Transactions on , Volume: 51 , Issue: 2 , April 2000

Pages:501 - 506

[Abstract] [PDF Full-Text (304 KB)] IEEE JNL

3 Optical fiber stress-location measurement by synthesis of binary optical coherence function

Hotate, K.; Kuramoto, A.; Zuyuan He;

Photonics Technology Letters, IEEE , Volume: 16 , Issue: 2 , Feb. 2004

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[Abstract] [PDF Full-Text (120 KB)] IEEE JNL

4 Polymer MEMS-based Fabry-Perot shear stress sensor

Fan-Gang Tseng; Chun-Jun Lin;

Sensors Journal, IEEE , Volume: 3 , Issue: 6 , Dec. 2003

Pages:812 - 817

[Abstract] [PDF Full-Text (1075 KB)] IEEE JNL

5 Stress Relaxation and Fatigue of Two Electromechanical Spring Mate Strengthened by Thermomechanical Processing*Fox, A.;*

Parts, Materials and Packaging, IEEE Transactions on , Volume: 7 , Issue: 1 , 1971

Pages:34 - 47

[\[Abstract\]](#) [\[PDF Full-Text \(1512 KB\)\]](#) [IEEE JNL](#)**6 Thin-Film Al-Al₂O₃-Al Capacitors***Martin, J.;*

Parts, Materials and Packaging, IEEE Transactions on , Volume: 1 , Issue: 1 , 1965

Pages:267 - 276

[\[Abstract\]](#) [\[PDF Full-Text \(1088 KB\)\]](#) [IEEE JNL](#)**7 Application of the Eyring Model to Capacitor Aging Data***Endicott, H.; Hatch, B.; Sohmer, R.;*

Component Parts, IEEE Transactions on , Volume: 12 , Issue: 1 , Mar 1965

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[\[Abstract\]](#) [\[PDF Full-Text \(1248 KB\)\]](#) [IEEE JNL](#)**8 A Photo-Patternable Stress Relief Material for Plastic Packaged Integrated Circuits***Cagan, M.; Ridley, D.;*

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[\[Abstract\]](#) [\[PDF Full-Text \(1576 KB\)\]](#) [IEEE JNL](#)**9 Reliability of Metallized Ceramic/Polyimide Substrates***Homa, T.; Posocco, A.;*

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Pages:396 - 402

[\[Abstract\]](#) [\[PDF Full-Text \(904 KB\)\]](#) [IEEE JNL](#)**10 Solder Attachment of Leaded Components to Thick Film Hybrids***Panousis, N.; Kershner, R.;*

Components, Hybrids, and Manufacturing Technology, IEEE Transactions on [also IEEE Trans. on Components, Packaging, and Manufacturing Technology, A, B, C] , Volume: 4 , Issue: 4 , Dec 1981

Pages:411 - 416

[\[Abstract\]](#) [\[PDF Full-Text \(1184 KB\)\]](#) [IEEE JNL](#)**11 Reliability Evaluation of Aluminum-Metallized MOS Dynamic RAM's**

Plastic Packages in High Humidity and Temperature Environments*Stringy, K.; Schelling, A.;*

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[\[Abstract\]](#) [\[PDF Full-Text \(832 KB\)\]](#) [IEEE JNL](#)**12 Role of Reliability and Accelerated Testing in VHSIC Technology***Malik, S.;*

Components, Hybrids, and Manufacturing Technology, IEEE Transactions on [also IEEE Trans. on Components, Packaging, and Manufacturing Technology, A, B, C] , Volume: 5 , Issue: 1 , Mar 1982

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[\[Abstract\]](#) [\[PDF Full-Text \(480 KB\)\]](#) [IEEE JNL](#)**13 Stress testing FET gates without the use of test patterns***Puri, Y.;*

Solid-State Circuits, IEEE Journal of , Volume: 10 , Issue: 5 , Oct 1975

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[\[Abstract\]](#) [\[PDF Full-Text \(448 KB\)\]](#) [IEEE JNL](#)**14 An Optimized and Reliable LDD Structure for 1-/spl mu/m NMOSFE Based on Substrate Current Analysis***Matsumoto, Y.; Higuchi, T.; Mizuno, T.; Sawada, S.; Shinozaki, S.; Ozawa, O.*
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Pages:349 - 353[\[Abstract\]](#) [\[PDF Full-Text \(736 KB\)\]](#) [IEEE JNL](#)**15 1.3 μ m buried heterojunction laser diodes under high electrical stress Leakage currents and aging behavior***Kuindersma, P.; Valster, A.; Baks, W.;*

Quantum Electronics, IEEE Journal of , Volume: 21 , Issue: 6 , Jun 1985

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[\[Abstract\]](#) [\[PDF Full-Text \(2992 KB\)\]](#) [IEEE JNL](#)[1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [11](#) [12](#) [13](#) [14](#) [15](#) [16](#) [17](#) [18](#) [19](#) [20](#) [21](#) [22](#) [23](#)
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